Serial No. 09/903,161
Docket : MIO 0076PA/40509.145

Amendments to the Specification:

Please replace the paragraph beginning at page 7, line 20, with the following amended paragraph.

The pins 110 of memory chip 104A couple to the circuit traces 108 in a manner such that the assignment of the circuit traces 108 external to the pins 110, that is $I_x(0)$ to $I_x(n)$, correspond to the identical internal pin assignment $I_i(0)$ to $I_i(n)$. That is, $I_x(0)$ couples to $I_i(0)$, $I_x(1)$ couples to $I_i(1)$ etc. all of the way around the chip 104A. However, because the corresponding chip 104B is connected to the circuit traces 108 on the reverse side of the wireboard substrate 102 (not shown in Fig. 3), the internal and external assignments will not correspond to identical bit positions. Rather, as illustrated in Fig. 3, $I_x(0)$ couples to $I_i(n)$, $I_x(1)$ couples to $I_i(n-1)$ etc. However, because all of the pins 110 couple to a like pin assignment function, that is, the signal on each pin assignment are all bits of the address or command buses respectively, the correct information can be received by either memory chip 104A or 104B by rerouting the logical information placed on the physical line or circuit trace 108. In other words, the logical information can be moved to a different physical circuit trace 108 so that the internal pin assignments receive the correct information regardless of whether the correct external assignment corresponding to a particular circuit trace is used. It shall be noted that for the purpose of this invention, the address and command pins are sufficiently ~~a like~~ alike that they can be interchanged.
